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Experimental Study of the Subsystems in a Microscale Additive Manufacturing Process

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High-throughput manufacturing of complex 3D architectures for microscale products such as microelectronics is limited by the resolution of existing additive manufacturing processes. This paper presents experimental testing and validation of the major subsystems in a microscale selective laser sintering (μ-SLS) process that is capable of fabricating true-3D metallic micro-architectures with microscale feature size resolutions. In μ-SLS, the part quality and throughput of the sintering process are largely determined by the precision, accuracy, and speed of the subsystems including: (1) the optical subsystem, (2) the global positioning mechanism, (3) the XY nanopositioning stage, and (4) the powder bed dispensing system. This paper shows that each of these subsystems can maintain the sub-micrometer precision and accuracy required to produce metal parts with microscale resolutions. Preliminary sintering results with optimized process parameters show the potential of the μ-SLS process to fabricate complex metal parts with sub-10-μm resolution at high rates.

INTRODUCTION

Additive manufacturing (AM) has been driving complex and innovative product design in the electronics, biomedical, and aerospace industries for the past few decades. Although most industrial applications of AM are specifically targeted towards rapid prototyping and replacements of non-critical parts, there has been a gradual shift towards large-scale direct manufacturing.[1–3] One of the leading areas of interest is additively fabricating microproducts and true-3D micro-architectures. The limitations posed by non-ideal geometries, process robustness, and overall throughput of existing micro-/nano-manufacturing techniques have spurred the need to explore alternative microscale AM processes. An interesting application of these processes is in microelectronics packaging. The 2D chip densities of semiconductor devices grow in line with the demand for high-performance computing and miniaturization. This leads to complex and long interconnect lines between chip components, which introduces significant R–C delays in processing speeds. 3D multi-module chip fabrication is a common solution to reduce interconnect lengths by vertical layer-by-layer integration of conducting and insulating layers. Conventional interconnect fabrication involves several steps including lithography (optical lithography/electron beam lithography), deposition, etching, and diffusion.[4,5] The high process complexity and low efficiencies of this procedure introduce several challenges in these back-end-of-line processes. AM provides an alternative to conventional chip fabrication and allows for true-3D integration capabilities. Unfortunately, most commercially available metal AM tools have minimum feature size resolutions of greater than 100 μm, which is too large to precisely produce interconnect structures for use in microelectronics packaging.[6]

One promising method of fabricating microscale parts out of metals with 3D structures is microscale sintering. Previous research on microscale laser-based sintering and melting techniques have primarily focused on producing microscale parts by scaling down traditional powder bed-based processes, such as selective laser melting or direct metal laser sintering by using thinner particle beds or smaller laser spot sizes. For example, Regenfuss et al.[7] presented a system using continuous wave

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lasers and q-switched pulsed lasers to develop high-resolution ($\sim$ 10 μm) parts with a 1.5-μm surface roughness. Similarly, Haferkamp et al.[8] developed a novel powder layer deposition technique where rollers moving in opposite directions were able to deposit powder layers of the order of tens of microns. However, these microscale sintering solutions run into problems when the desired feature size becomes less than 10 μm, and nanoscale powders are required to the microscale powders generally used in these systems. For example, particle agglomeration and write speed both become significant problems as the feature size is scaled down below 10 μm. Therefore, this paper presents the subsystems required for a novel microscale additive manufacturing process known as microscale selective laser sintering (μ-SLS), which is capable of producing 3D metal parts with sub-10-μm resolutions.

Figure 1 shows the designed assembly of the μ-SLS system which consists of the following subsystems: (1) the slot die coating subsystem to generate a uniform nanoparticle (NP) bed, (2) an optical system to direct and focus laser light to pattern features on to the bed, (3) a laser system to sinter the particles, (4) an XY nanopositioning system to step the bed under the optical system in order to enable large area patterning, and (5) a global travel system to position the substrate between the optical subsystem and the coating subsystem. Additional vibration isolation systems are used to reduce the external influences on the part fidelity.

Overall, the μ-SLS system works by first spreading a film of NP ink onto the build substrate using the slot die coating system and then drying the ink using the heated stage to form a thin layer of NPs. The air bearings and linear servo motor with feedback from the interferometric sensors is then used to precisely move the substrate under the optical subsystem. Once positioned under the optical system, a laser is focused off the DMD array down to a 2.3 $\times$ 1.3 mm pattern. Within this pattern, each pixel in the DMD is focused to a $\sim$ 1-μm spot allowing over 2 million 1-μm spots to be sintered simultaneously. The long-travel nanopositioning stage is used to move the substrate under the optical system in order to enable the precise patterning of the substrate over large areas. Once the first layer of the build has been patterned, the substrate is then brought back to the coating subsystem where a new layer of NPs is spread onto the substrate. The patterning and coating steps are then repeated as necessary in order to build up a part. Finally, once the build process is complete, the excess unsintered NPs are washed away in an ultrasonic bath leaving being just the final 3D μ-SLS part.

The design considerations for the subsystems within the μ-SLS process are aimed at addressing the following challenges process: (1) limited write speed due to small feature size, (2) uneven agglomeration of NPs within the powered bed resulting in poor feature resolution, (3) submicron motion precision and metrology, and (4) scalability of the process in a production environment.[3] To address these challenges, the primary design requirements of the μ-SLS system are as follows: (1) achieving a minimum feature size resolution of 1 μm, (2) spreading a uniform layer of metallic NP ink with submicron thicknesses, (3) aligning the sample under the optical subsystem with $<$ 200-nm tolerance before sintering each layer to achieve true-3D

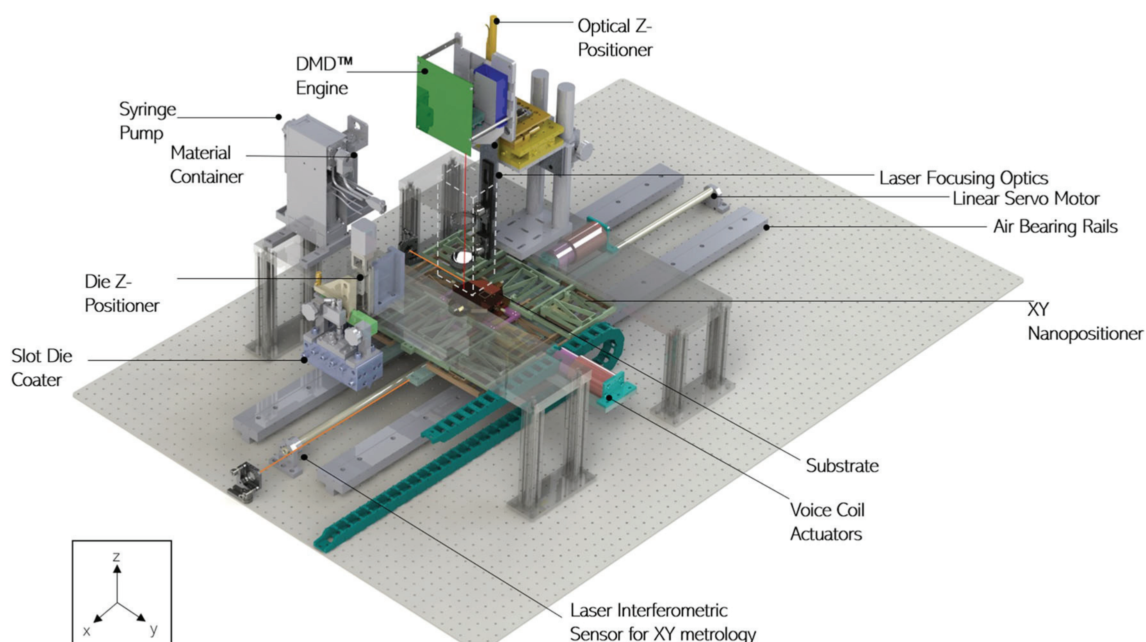


Fig. 1. CAD rendering of the microscale selective laser sintering system (μ-SLS) assembly.

structures, (4) fabricating near-net-shaped microscale features over a wafer size of 50 × 50 mm with a volumetric throughput of > 10 mm^3/h, and (5) identifying and measuring the sources of error within the subsystem and compensating for the errors. The following sections of this paper will examine the designs of each of the subsystems within the μ-SLS system and analyze how they address each of these design challenges to produce complex metal structures with microscale resolutions at high throughputs.

NANOPARTICLE INK BED DISPENSING MECHANISM

The first step in the μ-SLS process is the coating of the NPs onto the build substrate. In order to accomplish this task, the NP spreader mechanism in the μ-SLS assembly uses a slot die coating system to spread uniform layers of NP inks over the substrate. The system replaces the microscale powders used in conventional SLS processes with a NP ink to achieve the desired feature resolution. The use of nanoparticles in the μ-SLS system is necessary because, to build layers that are approximately 1 μm thick, it is necessary to use particles that are at least one order of magnitude smaller than the desired layer thickness. However, initial tests on spreading of Cu nanopowders demonstrated the formation of large agglomerates of NPs due to high van der Waals attraction between the NPs.[9] Therefore, the μ-SLS system uses NP inks to prevent the agglomeration of the NPs during the powder spreading process. NP inks provide solution to this agglomeration problem since they contain NPs that have a protective surfactant coating and are suspended in an organic solvent which reduces the van der Waals interaction between the particles and, hence, reduces the extent of agglomeration of the NPs in the bed. After spreading, a heated vacuum chuck is used to rigidly attach the substrate to the system and to dry the NP inks to produce the NP powder bed.

Slot coating is selected as the material deposition method in this process due to its ability to achieve high packing efficiencies in the sintered features and produce uniform layer-by-layer depositions. Other coating and printing processes for film formation are limited by high material wastage (spin coating, spray coating), low volumetric production rates (spin coating, vapor deposition), higher film thicknesses (slide coating, knife-over-edge coating), limited range of materials (ink jet printing, pad printing) and poor multiple layer deposition capabilities (spin coating, casting, screen printing).[10] The slot die coating subsystem consists of a precision machined aluminum die and a syringe pump for controlled and pre-metered dispense of the NP inks. The major sub-components of the slot die system include the positioning mechanism, the syringe pump, and the die assembly. The positioning mechanism translates the die head vertically to maintain a constant dispensing height for subsequent layer depositions. This positioning system consists of a precision ball screw linear rail with 3-μm positioning repeatability and backlash, driven by a 0.36° microstepping motor. A cylindrical flexural pivot along with a micrometer is used for in-plane positioning of the die head. A 60-mm stroke series syringe pump with a three-way rotary valve assembly is used as the metallic NP ink input source to the slot die coater, and a zero dead volume tip syringe driven by a precision ball screw ensures zero fluid carryover and complete purging of air bubbles from the system. The valve is operated by a NEMA 23 stepper motor to alternate the distribution and aspiration functions. The layout of the slot die coating system is presented in Fig. 2.

The primary requirement of the slot die coater is to facilitate the multiple layer coating capability by ensuring that new layers can be coated onto the substrate without distorting the existing layers underneath the coating. In addition to that, the slot die coater should be able to uniformly spread each layer of NP ink with submicron thicknesses. It is difficult to achieve sub-10-μm film thicknesses in the slot die coating process without having an accurate control over the gap between the slot die lips and the substrate.[11] This also introduces additional challenges at the design stage. The slot die lips need to be parallel to the substrate corresponding to the datum points. Assembly and machining tolerances affect the parallelism between the substrate and the die lips, which can lead to unwanted contact or crashes between the die and the substrate. Therefore, the first step in the coating process is to level the die with respect to the coating surface.

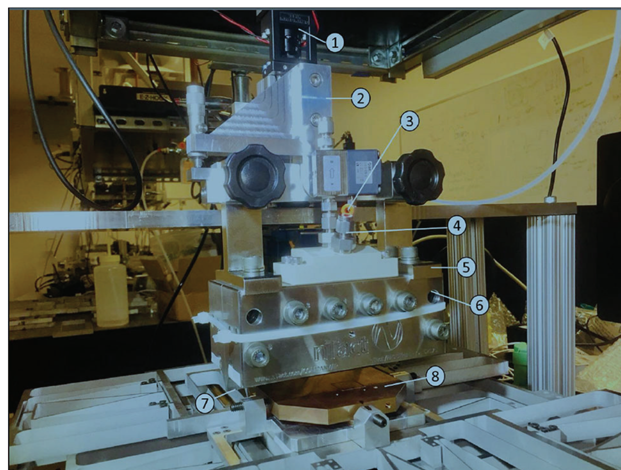


Fig. 2. Components in the assembly of the slot die coating system. (1) z-direction motor coupled with 100-mm travel leadscrew. (2) Pivoting bracket. (3) Input for air pilot valve. (4) Slot die input. (5) Die support arms. (6) Die head. (7) Die lips. (8) Substrate.

Once leveled, the slot die coating process involves initial priming of the fluid lines and the die with the NP ink. The die head design has a pneumatic air pilot valve which facilitates purging of entrapped air within the die. Figure 3 shows the average dried film thicknesses achieved for varying coating gaps. The flow rate into the die is varied from 2.5 to 5 mL/min and the coating speed is adjusted based on the coating gap to avoid low flow limits. The samples with a coating gap of 50 μm or 75 μm are coated at 10 mm/s while samples with a coating gap of 100 μm or 125 μm are coated at 15 mm/s. The thickness data are measured at multiple points along the direction of coating and across the width of the samples in order to generate uncertainty estimates in the coating thickness.

A functional requirement of the μ-SLS system is to fabricate 1-μm feature size resolutions. Preliminary results of the slot die coating system show that submicron layer thicknesses can be coated on a substrate to achieve the target resolution. For true-3D microelectronic parts, like vertical interconnects, thin layers of conductive inks can be coated and sintered on wafers in this manner.

GLOBAL TRAVEL

The global travel subsystem translates the substrate between the slot die coating station and the optical subsystem. The positioning accuracy of the global travel system needs to be better than 100 μm after which the XY nanopositioner positioning can take over and ensure that the sample is positioned with sub-200-nm accuracy. This level of positioning accuracy guarantees that the stack-up error between multiple build layers is significantly less than the 1-μm feature size resolution specification for the μ-SLS process. In addition, the global travel subsystem needs to ensure that the motion under the slot die coater is smooth and devoid of any hysteresis and backlash in order to obtain a uniform coating thickness under the slot die coater. In order to achieve these position accuracy and motion requirments, the global travel subsystem is designed with a non-contact linear motor to drive the translation and two air bearing rails to guide the motion. The linear motor consists of a slider assembly and a stator assembly. The slider is made of neodymium magnets encased in a precision-machined stainless steel tube. The stator has the motor windings and the position encoder along with sensors to actively monitor the motor health. The stator has several mounting options to secure the load. An internal encoder provides position feedback for the motor. The PID gains on the controller are tuned to achieve the best position and velocity feedback for the motor.

Figure 4 shows the positioning errors measured using the internal encoder in the linear actuator at different speeds in the coating region (240–360 mm from home position). The positioning accuracy is within 100 μm and increases with an increase in the linear velocity of the motor meeting the positioning requirements of this subsystem.

OPTICAL SUBSYSTEM

To meet the requirements of the μ-SLS process, the optical subsystem design needs to be able to achieve a feature size resolution of close to 1 μm while maintaining an areal throughput high enough to be used in a production environment. Generally, the volumetric throughputs required for microelectronics packaging applications are on the order of 10 mm^3/hr which translates into a required areal throughput of 3–4 mm^2/s assuming a 1 μm sintering layer thickness. Conventional sintering systems use triple-axis scanners, beam collimators, reflective mirrors and xy-galvanometric mirrors to produce a

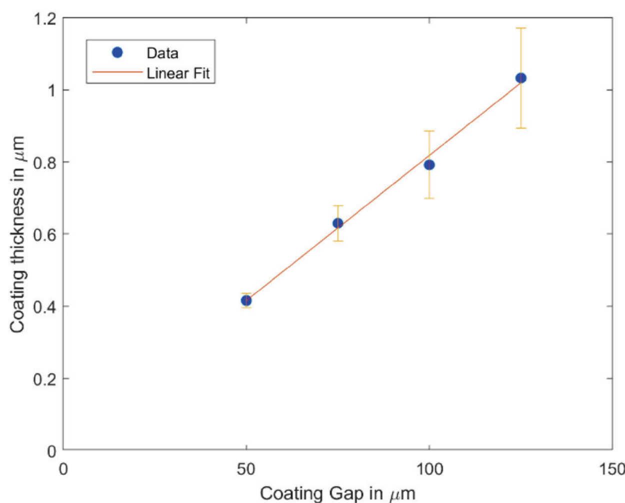


Fig. 3. Dry film coating thickness (in microns) versus coating gap (in microns) plot.

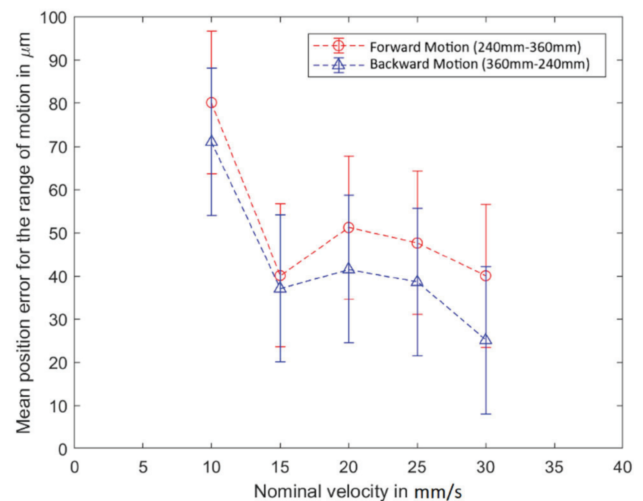


Fig. 4. Plot of the mean position error of the linear motor under applied load, toggling under the coating region in forward and backward directions at different velocities.

laser spot size of $\sim$ 100 μm.[6] However, if the spot size is reduced to 1 μm as required by μ-SLS, the process throughput decreases by a factor of 10^4. Therefore, to overcome this rate decrease, a digital micromirror device (DMD) is used in the μ-SLS system to project an image on the sintering plane so that multiple 1-μm spots can be sintered at once. This 1-μm feature size requirement also means that the diffraction-limited resolution of the imaging optics needs to be less than the 1-μm target resolution. The DMD uses a 1920 $\times$ 1080 array of MEMS mirrors with a 7.6-μm pitch and $\pm$ 12° tilt. The micromirrors either direct the light to a hermetically sealed converging lens when they are in the 'on' position or direct it to a heatsink during 'off' position, depending on the image being projected. An off-the-shelf optical solution to focus the light coming out of the DMD array is not able to minimize the loss of energy at the focal plane. Hence a high-efficiency custom-designed optical setup was used to focus the laser on the sample plane. Since the light coming out of the DMD diverges, a plano-convex collimating lens is placed axially in front of the DMD to make the beam of light parallel. The collimated light is then collected by using a converging lens to focus on to the sample plane with the desired resolution. The collimating lens diameter is sized to maximize the collection of light. To avoid the spherical aberration effect during the collimation of the beam, the plano-convex collimating lens is placed at a distance smaller than the focal length of the lens, which is selected to be 200 mm. The focusing lens is selected with the same diameter constraint along with a diffraction limited resolution of less than 1 μm. A 50-mm-diameter aspheric lens with a 30-mm focal length is selected as the focusing lens such that the size of each image at the focal plane is reduced by a factor of 200/30 = 6.66. The final focused image from the DMD array has a theoretical optical resolution of (7/6.66 μm) $\sim$ 1 μm.

The resolution of the optical subsystem is measured using a beam profiler to be 1.12 μm and the pattern size is measured to be 2.3 $\times$ 1.3 mm.[12] This shows that the current optical subsystem design is capable of achieving close to the targeted $\sim$ 1-μm desired resolution. Figure 5a shows the major components of the current optical setup and it can be observed that a vertical positioner is used to adjust the optical setup to get the best possible focusing at the sample plane. Additional alignment of the optical elements can be carried out to improve the focusing, and oto btain features with smaller heat-affected zones.

The optical system increases the throughput of the system, but the power requirement of the laser also increases significantly, given that the area being sintered is larger. Previous research has shown that the irradiance requirements for sintering on glass varies from 5000 to 12,000 W/cm^2, at 50-ms exposure, depending on the layer thickness.[13] The overall efficiency of the current optical system is 10%, due to losses in the optical elements inside the DMD and the alignment errors. Experiments with a continuous wave laser for sintering of Cu NPs showed that the irradiance requirements need to be higher than the sintering threshold. The maximum irradiance at the sample plane is around 500 W/cm^2, which means that the actual sintering must be carried out at longer exposure durations. A vacuum chuck with heating capabilities has been designed to heat the particle bed to an elevated temperature to reduce the energy requirements of the system and reduce the exposure durations. The wafer handling chuck is designed so as to allow for placement of thermoelectric heaters for heating of the wafer. The chuck design is symmetric with two plates: the top plate has slots for the wafer and vacuum lines and is heated using the Kapton heaters mounted on its underside. This top plate is held in place using four pin contacts on the four sides which are mounted from the bottom plate, as shown in Fig. 5b. This design allows for relief along the X and Y axes in-plane so that the warpage in the top plate is minimized when the sample is heated to the desired temperature. To minimize the thermal expansion effects and at the same time allow for fast heat conduction, an alloy of Cu, C145 tellurium Cu, which has a smaller coefficient of thermal expansion (16 ppm/°C) than either aluminum (24 ppm/°C) or copper (17.5 ppm/°C), with a thermal conductivity similar to Cu, is used for fabricating the chuck. FEA simulations have shown that the warpage in the optimized design with C145 alloy is smaller than both Cu and Al and other chuck designs, and is found to be less than 1 μm when the chuck is heated to 80–85°C.[14] Previous sintering experiments with a heated bed have also confirmed the hypothesis that heating the bed to a higher temperature significantly reduces the energy requirements for sintering of NPs,[15] as expected. Thus, the heated chuck design can be useful to the process in a number of ways: (1) lowering the energy requirements for sintering, (2) lower residual thermal stresses in the part, and (3) smaller heat-affected zones due to faster sintering.

XY NANOPOSITIONING STAGE

Once coarse positioning of the substrate has been achieved using the linear servo system, fine positioning can be achieved using the nanopositioning stage. A critical requirement of the nanopositioning stage is that it needs to be able to translate the sample under the optical system over a 50-mm range with > 10-Hz stepping speed in step-and-repeat fashion in order to be able to sinter the entire 50-mm wafer with the required throughput. Another requirement is that the nanopositioner be stepped under the optical station with sub-200-nm accuracy so that the overlay errors are minimized between different layers. Off-the-shelf nanopositioners are often limited by the range of motion or

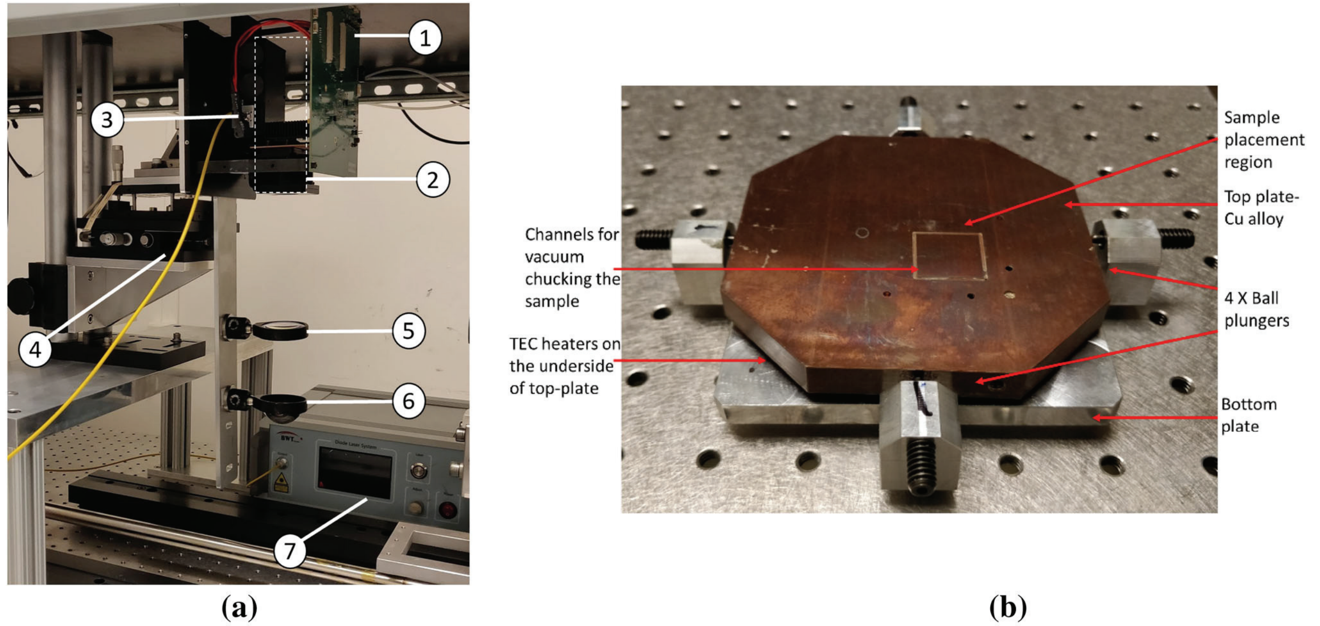


Fig. 5. (a) Optical subsystem assembly with the following components. (1) DMD controller board. (2) Primary optics and micromirror array (enclosed within a hermetically sealed housing). (3) Laser input. (4) Vertical positioning mechanism. (5) 50-mm-diameter plano-convex lens. (6) 50-mm-diameter aspheric lens. (7) 808-nm laser source. (b) Wafer chuck with heaters.

the motion quality, and those which meet both the range and motion quality requirements (such as air bearings and magnetic bearings) tend to be prohibitively expensive. An initial design of the XY nanopositioner by the authors used a double-parallelogram flexure mechanism (DPFM) to obtain the 50-mm motion range.[16] However, the resonant frequencies of the DPFM units, as predicted by the simulation and the observed during the experiments, were found to be in the 20–40 Hz range. This was primarily due to the additional degrees of freedom (DOFs) in the intermediate stages. To eliminate these unwanted DOFs, a modified stage was proposed which incorporated nested linkages inside the deadspace of the DPF bearing. The stages are actuated using voice coil actuators to provide frictionless strokes with fine force resolution. The detailed design, analytical modeling and fabrication techniques for both the stages have been presented in the work by Roy and Cullinan.[16]

The small displacement stiffness of the modified DPFM stage (see Fig. 6) is measured to be 1157 ± 162 N/m and the positioning noise in the stage is measured to be 106 ± 8 nm. Therefore, the stage is able to provide an open loop performance of a $\sim$ 100-nm motion resolution with a 1:1 signal to noise ratio. The parasitic motion range is found to be 1557 μm over the full range of travel which corresponds to 2.87% of the primary x-axis motion of the stage over a range of 54.29 mm. This represented a 20% improvement in the parasitic motion compared to the initial DPFM design. In addition, the parasitic motions are quite linear, allowing them to be removed through open-loop calibration of the motion. A modal analysis of the modified DPFM

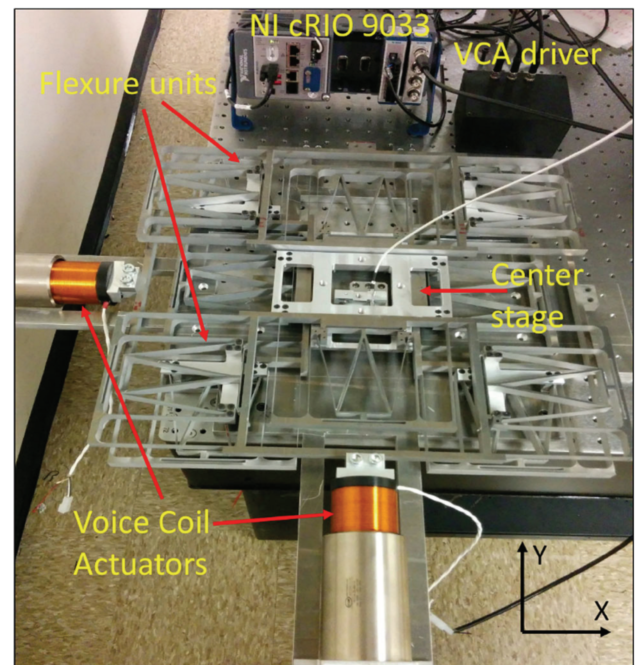


Fig. 6. Experimental setup used for XY stage characterization. (Adapted from Roy and Cullinan[16]).

showed that the first uncontrolled resonance mode is at 84.2 Hz, which is outside our range of operation. This has been further corroborated by experimental results.[16]

The long-range capability of the nanopositioning stage, however, comes at a cost, as it effectively increases the inertia of the stage, thereby decreasing the resonance frequency of the stage and the

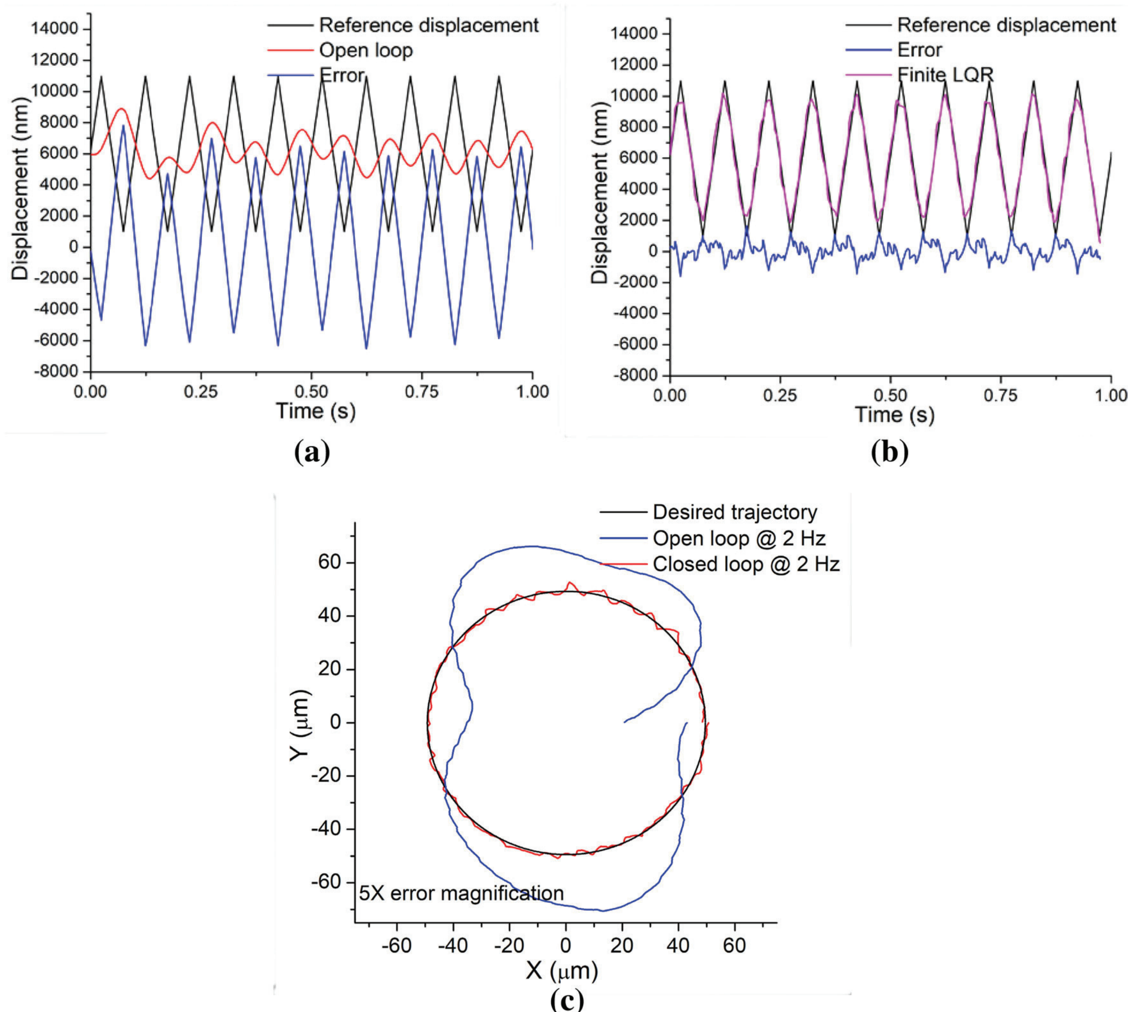


Fig. 7. Experimental triangular wave tracking comparison between (a) an open loop and (b) a closed loop at a frequency of 10 Hz, (c) XY stage tracking a 100-μm circle at 2 Hz in the open and closed loops with radial errors magnified 5 times for better visualization and comparison.

overall stepping speed. The stage is found to settle within 4% of the steady state value in 1.27 s, which hinders the high-throughput application needed in a μ-SLS system.[17] In addition to that, the low resonance frequency of the stage of 4.2 Hz and the low damping characteristics can excite the stage due to external disturbances (unwanted vibrations, people walking on the shop floor), and can substantially reduce the performance of the stage. To counter this, several closed-loop controller designs have been investigated to improve the positioning speeds while maintaining the positioning accuracy of the stage. A finite horizon linear quadratic regulator (LQR) controller, an infinite horizon LQR, and an integral resonant (IRC) controller were designed to track the nanopositioning stage. While the LQR and IRC controllers met the speed and tracking requirements of the μ-SLS system, the control effort required for the IRC controller was found to be two orders of magnitude higher than that required for the finite horizon LQR.[17] This makes its implementation in the actual systems more expensive, as higher force-rated actuators are required. Using the LQR controller, the positioning resolution of the stage was improved to 7.4 nm, and signals of up to 10 Hz can be effectively tracked. Figure 7a and b shows the stage tracking a 10-Hz triangular wave signal in a closed loop versus an open loop. As can be observed from this figure, the open loop tracking is poor and the errors in tracking are as large as 8 μm for the 5-μm amplitude signal. In the closed loop, the errors are reduced significantly, and the maximum error is within $\pm$ 1.5 μm. These maximum errors are found to occur at locations where the stage must reverse its direction and, hence, can be reduced even further by appropriate pre-compensation for the direction changes. For 2D tracking, the comparison between the open loop and the closed loop is depicted in Fig. 7c. The stage is tracking a 100-μm-diameter circle with a tracking speed of 2 Hz, and the radial errors for both the closed loop and the open loop are amplified 5 times for easier visualization and comparison between the two performances. The tracking speed

is defined as the number of circular patterns tracked in 1 s. These tests have been run multiple times and the mean radius of the circle in open loop is found to be 54.55 ± 0.09 μm, while the one standard deviation radial error for tracking is found to be 2024 ± 96 nm. With the closed loop control implementation, the mean radius of the tracked circle is much closer to the desired circle, with a radius of 49.64 ± 0.04 μm. Not only is the tracked circle much more accurate but it also has very precise tracking with a one standard deviation radial error of only 194 ± 28 nm, which is a ten times reduction in radial error compared to the open loop radial error. Overall, this error is an order of magnitude below the feature size resolution of the parts being built, showing that this stage with the LQR controller can be used to position the build substrate with the necessary speed and accuracy required for the μ-SLS process.

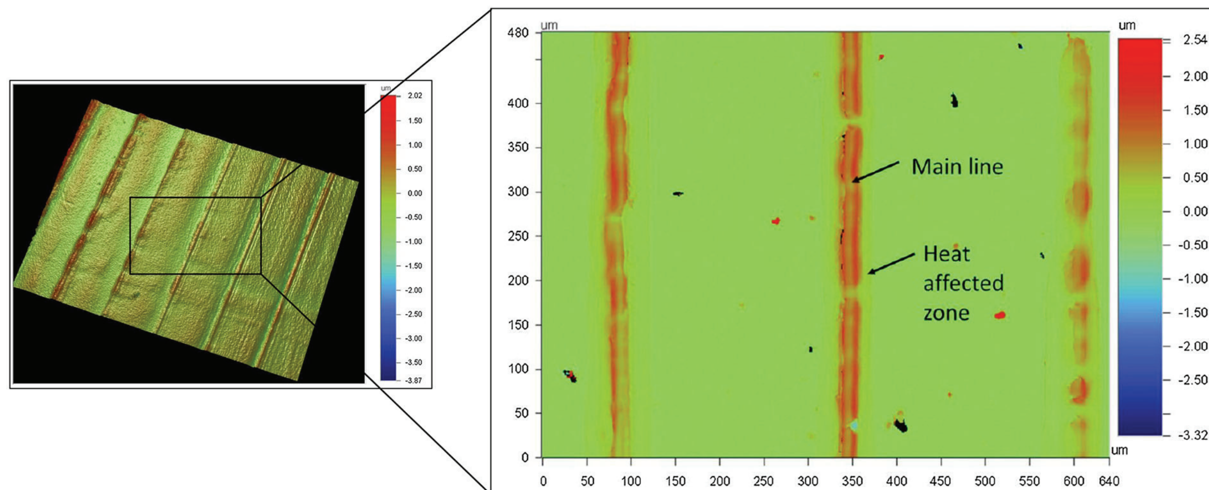
PRELIMINARY SINTERING RESULTS

In the preliminary sintering results presented in this paper, the NP ink is first slot die coated on the substrate and partially dried to remove excess solvent. The coated substrate is then translated to the optical station and aligned under the DMD micromirror array using the XY-nanopositioner. The image layer data are then sent to the DMD engine and the micromirrors are manipulated accordingly to either let the light through or redirect it to a heatsink. Next, the laser (50 W, 800 nm, CW laser) is turned on and the pattern is sintered. The XY-nanopositioner is used to step the NP-coated sample and sinter an array of patterns. After the first layer is sintered, the coating height is updated to lay down the second layer. The layer is partially dried again and then positioned under the optical station. An inline metrology step allows the XY-nanopositioner to align the substrate for the next layer. The process of sintering, coating, aligning and stepping is repeated until the desired aspect ratio is obtained. After the pattern is fabricated, the sample is ultrasonicated for 30–90 s (depending on the excess ink concentration). Using the base solvent for the inks, the excess ink can be recovered, thereby significantly reducing the material wastage.

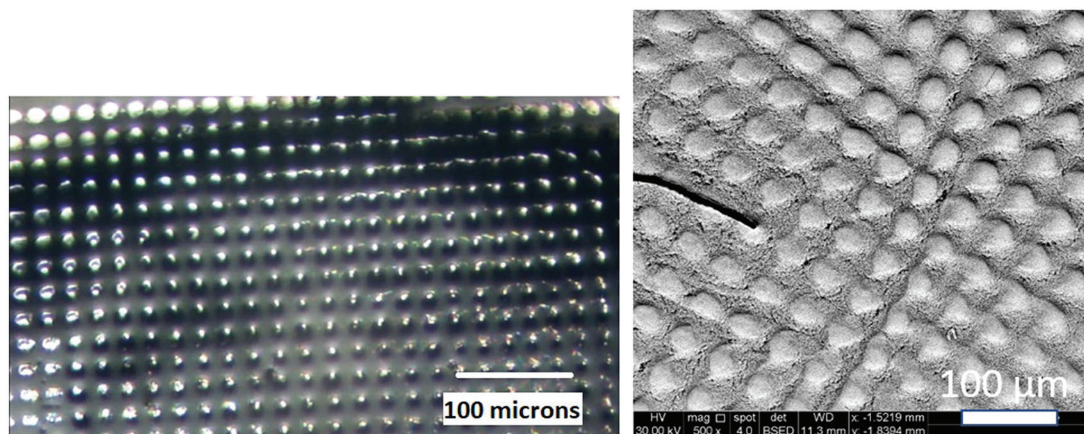
Figure 8a shows the optical profilometry results of a single-layer pattern with 10-μm line thicknesses with a 200-μm pitch. A closer identification of the pattern clearly shows the sintered line and the surrounding heat-affected zone. Figure 8b and c shows a single-layer array of 30-μm-diameter circles with a 40-μm pitch. The circular array corresponds to the vertical interconnects which can be sintered layer-by-layer. It demonstrates the feasibility of the process to be used for microelectronics packaging components such as solder bumps which are very difficult to produce with current electroplating technology beyond an aspect ratio of 2.[18] Figure 8d and e shows the complex patterning capability of the system, with a bitmap image and an optical microscope image of a single-layer sintered pattern, respectively, of the logo of the Nanoscale Design and Manufacturing Laboratory at UT-Austin. All these sintered patterns demonstrate the large area sintering capability of the system with a sub-10-μm feature resolution.

CONCLUSIONS AND FUTURE WORK

The μ-SLS tool employs a high-throughput, production-scale process which can be used in a variety of applications across the semiconductor, aerospace, and medical devices industries. In this study, we have presented brief descriptions of the different subsystems in this new micro-AM process. The different subsystems are designed and integrated to achieve the overall objective of producing parts with $<$ 10-μm feature size resolution for use in microelectronics packaging applications. The study presents a review of the design and performances of the individual subsystems that help in achieving the desired objectives of resolution and high throughput. The slot die coater is selected for particle bed generation due to its capability of spreading layers as thin as 100 nm to tens of microns and also because of its non-intrusive multiple-layer spreading capabilities. The system is shown to spread sub-micron layers of NPs with good consistency. The optical subsystem is designed to achieve $\approx$ 1-μm feature resolution with high areal throughput, and the sintering results demonstrated the large area sintering capability of the system along with fine feature resolution ($<$ 10 μm). An XY-nanopositioner has also been designed and shown to track signals up to 10-Hz frequency with a 50-mm travel range and sub-200-nm accuracy so as to maximize the throughput of the system with minimum registration errors. Additionally, a long linear servo-driven air bearing guide was also designed and tested for the long travel shuttling between the optical and spreader systems. Overall, the subsystems are shown to effectively meet their design requirements for their application in the μ-SLS process. Further optimization of the process parameters for various subsystems along with better process integration is expected to help in improving the feature resolution and robustness of the process. Future work will include integrating more precise stages for the alignment of lenses in the optical system that will enable us to improve the part feature resolution. In pursuit of smaller feature resolutions and heat-affected zones, a secondary energy source and a higher power primary laser source will be implemented to shorten the exposure durations for sintering. In addition, image correction algorithms will be implemented to correct for the heat spread in the bed due to conduction and improve feature resolution near sharp corners in parts.



(a)



(b) (c)

(d) (e)

Fig. 8. (a) Surface topography of a single-layer sintered sample with line thickness ~ 10 μm and line spacing ~ 200 μm. (b) Optical microscope image of a single layer, pre-ultrasonication sintered pattern with 30-μm-diameter circles and 40-μm pitch. (c) Scanning electron micrograph of the post-processed pattern with 30-μm-diameter circles and 40-μm pitch. (d) Bitmap image of the Nanoscale Design and Manufacturing Lab (NDML) logo, UT Austin, used as an input to the DLP chipset. (e) Optical microscope image of a single-layer, post-processed image of the NDML logo.

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